ensure a region outside of connection groove **125** to surely contact base region **30** and emitter electrode **90**.

[0119] As illustrated in FIG. **14**, the lower surface of gate electrode **60** facing the bottom surface of groove **25** may be tapered. Such a tapered lower surface of gate electrode **60** can reduce the area of the bottom surface of gate electrode **60** facing drift region **20** (collector region **10**) to reduce stray capacitance Cdg.

[0120] Groove **25** is filled with part of interlayer insulation film **70**. Accordingly, as illustrated in FIG. **14**, interlayer insulation film **70** may be formed such that the film thickness is large above the end of opening of groove **25** and is small above the central portion of opening of groove **25**. A large recess is generated above the central portion of opening of groove **25**, and in turn on the top surface of emitter electrode **90**. Such a configuration increases the connection area between emitter electrode **90** and clip lead or bonding wire arranged on the top surface of emitter electrode **90** to enhance connection strength.

[0121] If gate electrode **60** and bottom electrode **65** each are a polycrystalline silicon electrode containing a dopant, interlayer insulation film **70** preferably has a laminate structure of first insulation film **71** made of BPSG film and second insulation film **72** made of an NSG film as illustrated in FIG. **14**, for example. The BPSG film is an interlayer film whose surface can be smoothed by annealing while phosphorus (P) contained in the BPSG film affects the conductivity of the electrode. For this reason, the NSG film containing no phosphorus, as a protective film, can be arranged between the electrode and the BPSG film to attain a smooth top surface of interlayer insulation film **70** without affecting the conductivity of the electrode.

[0122] As illustrated in FIG. **14**, the interface between base region **30** and drift region **20** is located between grooves **25**, and the interface between base region **30** and drift region **20** in a region spaced from groove **25** is located at a lower level than the interface between base region **30** and drift region **20** in the region adjoining the grooves **25** (e.g., closer to collector region **10**). Such a configuration of the interface between base region **30** and drift region **20** increases a distance from the bottom of groove **25** to base region **30**. In such a configuration, drift region **20** can accumulate a larger amount of holes. The effect of conductivity modulation can be promoted to reduce on-resistance more significantly.

[0123] An n-type semiconductor region having a higher impurity concentration than that of drift region **20** may be arranged between drift region **20** and base region **30**. If such a semiconductor region having a high impurity concentration is arranged, drift region **20** accumulates a larger amount of holes in the vicinity of the interface between the semiconductor region and drift region **20** arranged thereunder. As a result, on-resistance can be reduced more significantly.

[0124] Apparently, the same effect can be attained if conductivity types (p-type and n-type) are inverted in the configuration above. Apparently, the structure and the production method described above can be implemented irrespective of materials for semiconductor substrate **100**, gate electrode **60**, and the like to attain the same effect.

[0125] As described above, to implement a semiconductor device having a carrier accumulation layer, the related techniques need a process of forming a carrier accumulation layer, which leads to an increase in the number of steps in production of the semiconductor device. Moreover, in the method of disposing a carrier accumulation layer having a higher impurity concentration than that of the semiconductor device in a drift region, the depletion layer does not expand well, and the trade-off between the breakdown voltage and the on-voltage cannot be sufficiently attained.

[0126] The applicants have found that the on-resistance can be reduced by increasing the width of the groove in IGBTs. Such an increase in the width of the groove in the structures of IGBTs, however, increases reverse transfer capacitance Crss.

[0127] The embodiment described above can sufficiently attain the trade-off between the breakdown voltage and the on-voltage, and provide a trench gate type semiconductor device having reduced reverse transfer capacitance.

[0128] Thus, the invention, off course, includes various embodiments which have not been described herein. Accordingly, the technical scope of the invention is determined only by particular matters of the invention according to the scope of claims.

[0129] The semiconductor device according to the invention can be used in applications of trench gate type semiconductor devices performing switching operation.

1. A semiconductor device comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type arranged on the first semiconductor region;

a third semiconductor region of the first conductivity type arranged on the second semiconductor region;

a fourth semiconductor region of a second conductivity type arranged on the third semiconductor region;

a groove extending from a top surface of the fourth semiconductor region and reaching the second semiconductor region through the fourth semiconductor region and the third semiconductor region;

an insulation film arranged on an inner wall of the groove,

a control electrode arranged on the insulation film at a side surface of the groove, the control electrode facing the third semiconductor region;

a connection groove connected to ends of the groove, the connection groove extending from the top surface of the fourth semiconductor region and reaching the second semiconductor region through the fourth semiconductor region and the third semiconductor region;

a first main electrode electrically connected to the first semiconductor region,

a second main electrode electrically connected to the fourth semiconductor region; and

a bottom electrode arranged on the insulation film at a bottom surface of the groove and spaced from the control electrode,

wherein the bottom electrode comprises a body arranged at the bottom surface of the groove and a connection portion electrically connected to the main body,

in plan view, the body is formed in a strip form, and extends in an extending direction of the groove, and the connection portion extends in a depth direction of the groove and is connected to an end of the body in the extending direction of the body,

the body of the bottom electrode is arranged in the groove, and the connection portion of the bottom electrode is arranged in the connection groove, and

in plan view, a length of the groove in the extending direction of the groove is larger than a width of the groove, and the width of the groove is larger than a gap between the groove and an adjacent groove.